WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a shared-scheme sense amplifier;

a bit line connected to the sense amplifier;

first and second select transistors arranged on both sides of the sense amplifier and connected to the bit line;

a first memory cell array connected to the bit line via the first select transistor, the first memory cell array including a plurality of memory cells each having a cell transistor and a ferroelectric capacitor;

a second memory cell array connected to the bit line via the second select transistor, the second memory cell array including a plurality of memory cells each having a cell transistor and a ferroelectric capacitor;

a setting circuit which controls the first and second select transistors, thereby setting the first and second memory cell arrays in an operative state at the same time; and

a control circuit which performs a test at the same time for the first and second memory cell arrays, which are set in the operative state at the same time by the setting circuit.

2. A semiconductor memory device according to claim 1, wherein the control circuit controls, during a fatigue test, a potential difference between the

ferroelectric capacitors included in memory cells to be tested of the plurality of memory cells.

3. A semiconductor memory device according to claim 1, wherein the bit line comprises a signal line pair.

4. A semiconductor memory device according to claim 1, wherein a word line is connected to a gate terminal of each cell transistor.

5. A semiconductor memory device according to claim 1, wherein each of the first and second memory cell arrays includes a plurality of memory blocks, each of the plurality of memory blocks being formed by connecting a predetermined number of the plurality of memory cells in series, one terminal of each of the plurality of memory blocks being connected to the bit line via a block select transistor, and the other terminal of each of the plurality of memory blocks being connected to a plate line.

6. A semiconductor memory device according to claim 5, wherein each of the plurality of memory cells is configured such that a ferroelectric capacitor is connected in parallel between a source and a drain of the cell transistor.

7. A semiconductor memory device according to claim 1, wherein each of the first and second memory cell arrays includes the plurality of memory cells, each of which is configured such that one end of a

ferroelectric capacitor is connected in series to one of a source terminal and a drain terminal of the cell transistor.

8. A semiconductor memory device according to claim 7, wherein each of the plurality of memory cells is configured such that the other of the source and drain terminals of the cell transistor is connected to the bit line, and the other end of the ferroelectric capacitor is connected to a plate line.

9. A method of testing a semiconductor memory device including:

first and second select transistors arranged on both sides of a shared-scheme sense amplifier and connected to a bit line;

a first memory cell array connected to the bit line via the first select transistor, the first memory cell array including a plurality of memory cells each having a cell transistor and a ferroelectric capacitor;

a second memory cell array connected to the bit line via the second select transistor, the second memory cell array including a plurality of memory cells each having a cell transistor and a ferroelectric capacitor,

the method comprising:

controlling the first and second select transistors by a setting circuit, thereby setting the first and second memory cell arrays in an operative

state at the same time; and

performing a test at the same time, by a control circuit, for the first and second memory cell arrays, which are set in the operative state at the same time by the setting circuit.

10. A method of testing a semiconductor memory device according to claim 9, wherein the control circuit controls, during a fatigue test, a potential difference between the ferroelectric capacitors included in memory cells to be tested of the plurality of memory cells.

11. A method of testing a semiconductor memory device according to claim 9, wherein each of the first and second memory cell arrays includes a plurality of memory blocks, each of the plurality of memory blocks being formed by connecting a predetermined number of the plurality of memory cells in series, one terminal of each of the plurality of memory blocks being connected to the bit line via a block select transistor, the other terminal of each of the plurality of memory blocks being connected to a plate line, each of the plurality of memory cells being configured such that a ferroelectric capacitor is connected in parallel between a source and a drain of the cell transistor, and a word line being connected to a gate terminal of each cell transistor,

wherein during a fatigue test the control circuit

alternately changes the potential of the bit line and the potential of the plate line in a state in which the word line associated with memory cells to be tested of the plurality of memory cells is selected and all the block select transistors are selected.

12. A method of testing a semiconductor memory device according to claim 11, wherein the control circuit controls the potential of the bit line by setting a first control transistor connected to the bit line in a conductive state, and by applying a pulse signal to a source of the first control transistor.

13. A method of testing a semiconductor memory device according to claim 11, wherein the control circuit controls the potential of the bit line by raising the potential of the bit line up to a power supply potential using a second control transistor connected to the bit line, and by lowering the potential of the bit line to a ground potential using a third control transistor connected to the bit line.

14. A method of testing a semiconductor memory device according to claim 9, wherein each of the first and second memory cell arrays includes a plurality of memory blocks, each of the plurality of memory blocks being formed by connecting a predetermined number of the plurality of memory cells in series, one terminal of each of the plurality of memory blocks being connected to the bit line via a block select

transistor, the other terminal of each of the plurality of memory blocks being connected to a plate line, each of the plurality of memory cells being configured such that the ferroelectric capacitor is connected in parallel between a source and a drain of the cell transistor, and a word line being connected to a gate terminal of each cell transistor,

wherein during a fatigue test, a read operation for memory cells to be tested of the plurality of memory cells is executed in a state in which the word line and the block select transistors associated to the memory cells to be tested are selected.

15. A method of testing a semiconductor memory device according to claim 9, wherein each of the first and second memory cell arrays includes the plurality of memory cells, each of which is configured such that one end of a ferroelectric capacitor is connected to one of a source terminal and a drain terminal of the cell transistor, each of the plurality of memory cells is configured such that the other of the source and drain terminals of the cell transistor is connected to the bit line and the other end of the ferroelectric capacitor is connected to a plate line, and a word line is connected to a gate terminal of each cell transistor,

wherein during a fatigue test the control circuit alternately changes the potential of the bit line and

the potential of the plate line in a state in which all the word lines are selected.

16. A method of testing a semiconductor memory device according to claim 15, wherein the control circuit controls the potential of the bit line by setting a first control transistor connected to the bit line in a conductive state, and by applying a pulse signal to a source of the first control transistor.

17. A method of testing a semiconductor memory device according to claim 15, wherein the control circuit controls the potential of the bit line by raising the potential of the bit line up to a power supply potential using a second control transistor connected to the bit line, and by lowering the potential of the bit line to a ground potential using a third control transistor connected to the bit line.

18. A method of testing a semiconductor memory device according to claim 9, wherein each of the first and second memory cell arrays includes the plurality of memory cells, each of which is configured such that one end of a ferroelectric capacitor is connected to one of a source terminal and a drain terminal of the cell transistor, each of the plurality of memory cells is configured such that the other of the source and drain terminals of the cell transistor is connected to the bit line and the other end of the ferroelectric capacitor is connected to a plate line, and a word line

is connected to a gate terminal of each cell transistor,

wherein during a fatigue test a read operation for memory cells to be tested of the plurality of memory cells is executed in a state in which the word line associated to the memory cells to be tested is selected.